	Type	L #	Hits	Search Text	DBs
1	BRS	L1	0	shin near jiaw-ren.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L2	104	lee near jian-hsing.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L3	49	chen near shui-hung.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	33	((doped-well) or (doped near well)) near25 (polarity)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
5	BRS	L5	1214	((doped-well) or (doped near well)) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L6	168	((doped-well) or (doped near well)) near25 (wafer or substrate) near60 (oxide)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L7	19	((third) near5 ((doped-well) or (doped near well))) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L8	6	((third) near ((doped-well) or (doped near well))) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
9	BRS	L9	0	((metal near oxide) near ((doped-well) or (doped near well))) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
10	BRS	L10	36	((metal near oxide) near ((doped-well) or (well))) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
11	BRS	L11	1341	((metal near oxide) near35 (well)) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
12	BRS	L12	5	((metal near oxide) near35 (well)) near25 (polarity) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
13	BRS	L13	1214	((doped-well) or (doped near well)) near25 (wafer or substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	U	1	Document ID	Title
1			US 20050041070 A1	LDMOS and CMOS integrated circuit and method of making
2			US 20040051147 A1	Method for making high-gain vertical bipolar junction transistor structures compatible with CMOS process
3			US 20020109202 A1	Diode structure on MOS wafer
4			US 6818494 B1	LDMOS and CMOS integrated circuit and method of making
5			US 6630377 B1	Method for making high-gain vertical bipolar junction transistor structures compatible with CMOS process
6			US 6465864 B2	Diode structure on MOS wafer